WHAT IS CLAIMED IS:

1. A solid state image sensor comprising a plurality of amplifying unit pixels arranged two-dimensionally on a semiconductor substrate, each of said plurality of amplifying unit pixels including a photoelectric conversion region for subjecting incident light to photoelectric conversion; a read transistor for reading signal charge obtained through the photoelectric conversion; a storage region for storing said signal charge read by said read transistor; a detect transistor for detecting said signal charge on the basis of application of potential of said storage region to a gate thereof; a reset transistor for resetting said signal charge stored in said storage region; and a drain region for supplying a pulse voltage to said storage region through said reset transistor,

wherein a read pulse for said read transistor of a first pixel out of said plurality of amplifying unit pixels and a reset pulse for said reset transistor of a second pixel adjacent to said first pixel in a column direction are supplied through a common gate line,

a LOW level potential of said drain region of said first pixel is set, in resetting said second pixel, to a potential higher than a potential depth of said photoelectric conversion region of said first pixel.

2. The solid state image sensor of Claim 1,

wherein potential below a gate of said reset transistor of said first pixel obtained by applying a LOW level voltage to said gate is set to a potential higher than the LOW level potential of said drain region of said first pixel.

3. A solid state image sensor comprising a plurality of amplifying unit pixels arranged two-dimensionally on a semiconductor substrate, each of said plurality of amplifying unit pixels including a photoelectric conversion region for subjecting incident light to photoelectric conversion; a read transistor for reading signal charge obtained through the photoelectric conversion; a storage region for storing said signal charge read by said read transistor; a detect transistor for detecting said signal charge on the basis of application of potential of said storage region to a gate thereof; a reset transistor for resetting said signal charge stored in said storage region; and a drain region for supplying a pulse voltage to said storage region through said reset transistor,

wherein a read pulse for said read transistor of a first pixel out of said plurality of amplifying unit pixels and a reset pulse for said reset transistor of a second pixel adjacent to said first pixel in a column direction are supplied through a common gate line,

a LOW level potential of said drain region of said first pixel is set, in resetting said second pixel, to a

potential lower than a potential depth of said photoelectric conversion region of said first pixel.

4. The solid state image sensor of Claim 3,

wherein potential below a gate of said reset transistor of said first pixel obtained by applying a LOW level voltage to said gate is set to a potential higher than the LOW level potential of said drain region of said first pixel.

5. A solid state image sensor comprising a plurality of amplifying unit pixels arranged two-dimensionally on a semiconductor substrate, each of said plurality of amplifying unit pixels including a photoelectric conversion region for subjecting incident light to photoelectric conversion; a read transistor for reading signal charge obtained through the photoelectric conversion; a storage region for storing said signal charge read by said read transistor; a detect transistor for detecting said signal charge on the basis of application of potential of said storage region to a gate thereof; a reset transistor for resetting said signal charge stored in said storage region; and a drain region for supplying a pulse voltage to said storage region through said reset transistor,

wherein a read pulse for said read transistor of a first pixel out of said plurality of amplifying unit pixels and a reset pulse for said reset transistor of a second pixel adjacent to said first pixel in a column direction are

supplied through a common gate line, and

a LOW level voltage applied to a gate of said read transistor of each pixel is set to voltage lower than a LOW level voltage applied to a gate of said reset transistor thereof.

6. The solid state image sensor of any of Claims 1 through 5, further comprising:

a vertical shift register for selecting one row of said plurality of amplifying unit pixels; and

a circuit for generating said read pulse for said first pixel by using an output from one stage of said vertical shift register, generating said reset pulse for said second pixel by using an output from another following stage of said vertical shift register, and supplying a signal corresponding to a logical OR of said generated read pulse and reset pulse to said common gate line.

7. The solid state image sensor of Claim 6,

wherein said circuit includes two AND circuits and wired OR connection of outputs of said two AND circuits,

each of said two AND circuits includes:

a capacitor;

a switch for applying a first signal to a first end of said capacitor for charging said capacitor;

means for applying a second signal to a second end of said capacitor; and

a transistor for preventing reverse flow with a gate thereof connected to said first end of said capacitor, a drain thereof connected to said second end of said capacitor and a source thereof connected to a node of said wired OR connection.

8. The solid state image sensor of any of Claims 1 through 5,

wherein said drain regions of said plurality of amplifying unit pixels are connected to different drain lines row by row and said detect transistors of said plurality of amplifying unit pixels are connected to different signal lines column by column, and

said drain line and said signal line are disposed to cross each other in different layers.

9. The solid state image sensor of Claim 8, further comprising:

a vertical shift register for selecting one row of said plurality of amplifying unit pixels;

a first circuit for generating said read pulse for said first pixel by using an output from one stage of said vertical shift register, generating said reset pulse for said second pixel by using an output from another following stage of said vertical shift register and supplying a signal corresponding to a logic OR of said generated read pulse and reset pulse to said common gate line on a corresponding row;

and

a second logic circuit for supplying, to said drain line on a corresponding row, a power pulse generated by using the output from the same stage of said vertical shift register as that used in generating said read pulse.

10. The solid state image sensor of Claim 8,

wherein said gate line and said drain line are formed in the same interconnect layer.

11. The solid state image sensor of Claim 8,

wherein a line for connecting said storage region to a gate of said detect transistor is made from a first light blocking metal layer.

12. The solid state image sensor of Claim 8,

wherein a line for connecting said storage region to a gate of said detect transistor and said drain line are made from a first metal layer above said gate line, and

said signal line is made from a second metal layer above said first metal layer.

13. The solid state image sensor of Claim 8,

wherein a line for connecting said storage region to a gate of said detect transistor and said signal line are made from a first metal layer above said gate line, and

said drain line is made from a second metal layer above said first metal layer.

14. A solid state image sensor comprising a plurality

of amplifying unit pixels arranged two-dimensionally on a semiconductor substrate, each of said plurality of amplifying unit pixels including a photoelectric conversion region for subjecting incident light to photoelectric conversion; a read transistor for reading signal charge obtained through the photoelectric conversion; a storage region for storing said signal charge read by said read transistor; a detect transistor for detecting said signal charge on the basis of application of potential of said storage region to a gate thereof; a reset transistor for resetting said signal charge stored in said storage region; and a drain region for supplying a pulse voltage to said storage region through said reset transistor,

wherein a read pulse for said read transistor of a first pixel out of said plurality of amplifying unit pixels and a reset pulse for said reset transistor of a second pixel adjacent to said first pixel in a column direction are supplied through a common gate line,

a potential of said drain region of said first pixel is set to a HIGH level potential when said second pixel is reset and is set to a LOW level potential when said signal charge obtained through the photoelectric conversion is read by said read transistor to said storage region so as to operate said detect transistor in said second pixel, and

potential below a gate of said reset transistor of said

first pixel obtained by applying a LOW level voltage to said gate is set to a potential higher than a potential depth of said photoelectric conversion region of said first pixel.

15. The solid state image sensor of Claim 14,

wherein said HIGH level potential of said drain region is zero.

16. A solid state image sensor comprising a plurality of amplifying unit pixels arranged two-dimensionally on a semiconductor substrate, each of said plurality of amplifying unit pixels including a photoelectric conversion region for subjecting incident light to photoelectric conversion; a read transistor for reading signal charge obtained through the photoelectric conversion; a storage region for storing said signal charge read by said read transistor; a detect transistor for detecting said signal charge on the basis of application of potential of said storage region to a gate thereof; a reset transistor for resetting said signal charge stored in said storage region; and a drain region for supplying a voltage for resetting said signal charge stored in said storage region through said reset transistor,

wherein said drain regions of said plurality of amplifying unit pixels are connected to a single drain layer also working as a light blocking film.